

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of: **Andreas C. DOERING et al.**

Serial No.: **To Be Assigned**

Filed: **Herewith**

Title: **METHOD AND APPARATUS FOR USING FPGA TECHNOLOGY WITH A MICROPROCESSOR FOR RECONFIGURABLE, INSTRUCTION LEVEL HARDWARE ACCELERATION**

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT (IDS) UNDER 37 CFR 1.97

Dear Sir:

Applicants submit herewith patents, publications or other information which they are aware, which they believe may be material to the patentability of this application and in respect of which there may be a duty to disclose in accordance with 37 CFR 1.56.

While this Information Disclosure Statement may be "material" pursuant to 37 CFR 1.56, it is not intended to constitute an admission that any patent, publication or other information referred to herein is "prior art" for this invention unless specifically designated as such.

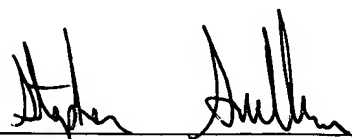
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This Information Disclosure Statement is being submitted with only copies of non-U.S. patent publication(s) and non-patent literature. This protocol conforms with 37 CFR 1.98(a)(2)(i), which waives the requirement for submitting a copy of each cited U.S. Patent and each U.S. patent application publication for all U.S. national patent applications filed after June 30, 2003.

Respectfully submitted,

10/29/03
Date

By:


Stephen G. Sullivan
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Registration No. 38,329

FORM PTO-1449 (Modified) LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY. DOCKET NO. RPS920030110US1	SERIAL NO. To Be Assigned
	APPLICANT: Andreas DOERING et al.	
	FILING DATE: Herewith	GROUP: To Be Assigned

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

EXAMINER INITIALS		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)
		US 2002/0008549	01/24/02	Britton et al.	326	40	
		US 2002/0100029	07/25/02	Bowen	717	140	
		US 2002/0133725	09/19/02	Roy et al.	713	202	
		US 2002/0174411	11/21/02	Feng et al.	716	12	
		US 2002/0188885	12/12/02	Sihlbom et al.	713	600	
		US 2003/0025132	02/06/03	Tobey	257	202	
		US 2003/0056084	03/20/03	Holgate et al.	712	29	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

		Borgatti, Michele et al., "A Reconfigurable System Featuring Dynamically Extensible Embedded Microprocessor, FPGA, and Customizable I/O," IEEE Journal of Solid-State Circuits, Vol. 38, No. 3, March 2003, pp. 521-529.
		Hauser, John R. et al., "Garp: A MIPS Processor with a Reconfigurable Coprocessor," IEEE 1997, pp. 12-21.

EXAMINER

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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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EXAMINER INITIALS		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)
		5 9 3 7 1 7 9	08/10/99	Swoboda	395	500	
		6 0 4 1 1 4 0	03/21/00	Binns et al.	382	209	
		6 4 6 7 0 0 9	10/15/02	Winegarden et al.	710	305	
		6 5 0 4 3 9 8	01/07/03	Lien et al.	326	41	
		6 5 0 4 3 9 9	01/07/03	Pani et al.	326	41	

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